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Study on crystallization mechanism of GeSn interlayer for low temperature Ge/Si bonding

Ziwei Wang[1], Ziqi Zhang[1], Donglin Huang[1], Shaoying Ke[2], Zongpei Li[1], Wei Huang[1], Jianyuan Wang[1], Cheng Li[1], and Songyan Chen[1,*]

[1] *Department of Physics, Department of Electronic Engineering and Jiujiang Research Institute, Xiamen University, Xiamen 361005 China*

[2] *College of Physics and Information Engineering, Minnan Normal University, Zhangzhou 363000 People's Republic of China*

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ABSTRACT

Low temperature bonding technologies is necessary in next-generation photonic integrated circuits, such as flexible optoelectronic devices, low dark current Ge/Si devices and so on. Since Germanium-Tin (GeSn) alloy has lower crystallization temperature, in this work, amorphous GeSn with 5% Sn alloy by magnetron sputtering is introduced as an intermediate layer for wafer bonding innovatively. And high strength Ge/Si heterojunction with a crystal GeSn layer is realized without any surface activation process. Two mechanisms in the interlayer crystallization are put forward and substantiated experimentally and theoretically: (1) the a-GeSn turns to be poly-GeSn due to the induction of the c-Ge substrate. (2) Stress between Si wafer and interlayer due to thermal mismatch contributes to the crystallization. It is concluded that GeSn semiconductor interlayer bonding would be one of the potential technologies for bonding process.

1 Introduction

Wafer bonding plays an important role not only in Micro-Electronic-Mechanical-System (MEMS) integrated packaging [1, 2], but also in homojunctions [3] and heterojunctions [4]. Compared with traditional epitaxial growth, wafer bonding can effectively avoid threading dislocations (TDs) in the Ge film due to high lattice mismatch and thermal mismatch for Ge/Si, such as Ge/Si single-photon avalanche photodiodes (APD) [5]. On the other hand, with recent advances in flexible photonic applications, direct bonding and transfer printing technology is a promising way to achieve excellent mechanical flexibility and material quality. For example, there are flexible Si nano-film (NM) phototransistors with a back gate configuration [6], the strained GeSn metal-semiconductor-metal (MSM) photodetectors (PDs) on polyethylene terephthalate (PET) substrates [7]. Generally flexible substrates can't bear high temperature, hence lower temperature bonding is necessary.

To date, the widely used methods in wafer bonding are mainly focus on hydrophilic wet wafer bonding, hydrophobic wet wafer bonding, plasma-

Address correspondence to E-mail: sychen@xmu.edu.cn

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activated bonding, high-vacuum surface-activated bonding, dry wafer bonding, and semiconductor interlayer bonding [8]. More recently, p-Ge/n-Si integration was fabricated by wafer bonding and layer exfoliation with a low thermal budget [9]. While plasma-activated bonding introduces dangling bonds at the bonded interface, resulting in very large surface leakage current. Further, Liu et al. achieved Ge/Si micro-ribbon bonding with a process temperature as low as 150 °C [10]. However, the forward current of this device does not improve significantly because of trap induced mechanism and inter-band tunneling. An oxide layer 3∼5 nm at the bonded interface is harmful for fabricating high-performance Ge/Si devices. Therefore semiconductor interlayer bonding is promising to obtain Ge/Si wafers without an oxidation layer [11] in 400 °C. Conventionally, the intermediate bonding layer consisting of gold-tin (Au–Sn) [12], gold-germanium (Au-Ge) [13] or gold-silicon (Au–Si) [14] is easy to realize eutectic bonding by change melt temperature. Thus far, this method is mainly used in high-temperature power devices [15], but not supportable for most optoelectronic devices [16, 17] due to the high cost and thermo-compression process.

Based on the above problems, amorphous GeSn is innovatively introduced as an intermediate layer for Ge/Si wafer bonding in this work. On the one hand, due to the low crystallization temperature (300 °C) and unique crystallization mechanism of GeSn, high bonding strength and oxide-layer-free interface are achieved, demonstrating the potential of GeSn interlayer for low temperature Ge/Si wafer bonding. On the other hand, bonded wafers structure prevents Sn segregation from GeSn film, which provides guidelines to synthesizing GeSn with high Sn composition. Samples of Ge/a–GeSn/Si, Ge/a–Ge/Si, Si/GeSn/Si were prepared to explore the influencing factors of improving bonding quality. Based on C-mode scanning acoustic microscope (CSAM), Scanning electron microscope (SEM), Raman spectroscopy (Raman), Transmission electron microscope (TEM), bonding strength tests and finite element simulation analysis, the relationship between the crystallinity of GeSn regions and bonding strength, and the mechanism of stress-induced crystallization are investigated.

2 Experiment

4 inches of (100) n-Si substrates (∼ 5 Ω·cm) and (100) i-Ge substrates were cut into 1 cm×2 cm slices. The Ge slices were degreased with acetone, alcohol, and deionized water in the ultrasonic bath for 10 min, respectively. The Si slices were chemically cleaned with the standard RCA process and organic solutions. Subsequently, the Ge slices were loaded into a three-target magnetron sputtering system (TRP-450) to depositing a-GeSn. In order to minimize the crystallization temperature with an acceptable bonding quality, a-$Ge_{0.95}Sn_{0.05}$ was selected as the bonding interlayer. When ambient pressure is pumped to10^{-4} Pa, the 45 nm-thick a-$Ge_{0.95}Sn_{0.05}$ films were deposited at room temperature in atmosphere of pure argon by DC magnetron co-sputtering Sn and Ge targets for 130 s. The power ratio is 120 w: 3 w. The root mean square roughness (RMS) of the film was controlled below 0.5 nm, which is essential to ensure the cohesion of direct bonding.

Subsequently, take the Ge slices out of the chamber and bonded to Si. Three Ge/$Ge_{0.95}Sn0._{05}$/Si samples were subjected to tube furnace and annealed at 200 °C, 300 °C, 400 °C for 20 h separately to enhance bonding strength. No pressure was applied on the wafers during annealing. The schematic flow of Ge/Si bonding are shown in Fig. 1. In order to systematically investigate the influence of different structure towards bond strength, Ge/a-Ge/Si bonded wafers and Si/a–$Ge_{0.95}Sn_{0.05}$/Si bonded wafers were also prepared by the same method.

The quality of bonding chips was examined by CSAM from SAM 301 (PVA TePla) with an acoustic head frequency at 230 MHz, SEM and high-resolution transmission electron microscope (HRTEM). Bonded wafers were cut into 1 cm × 1 cm and then glued onto hooks. Then, the AGS-X 5KN electronic universal testing machine is applied to test the bonding strength. The strength calculation formula is P = F/S, where F is the tension obtained by the test, S the area of the bonded wafers. The crystallinity of intermediate layer was characterized by laser Raman spectroscopy (488 nm laser) after pulling apart the bonded samples.

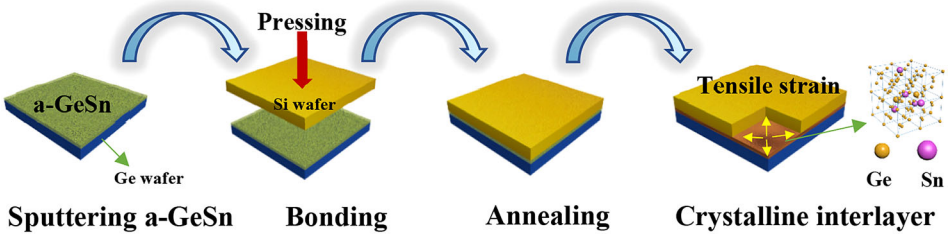

Fig. 1 Schematic flow of Ge/Si bonding via deposition of ultra-thin GeSn film

2.1 Results and discussion

A comparison of Ge/Si wafers after annealing at 200 °C, 300 °C and 400 °C has been performed. Figure 2a–c shows CSAM pictures of bonded pairs. The black areas represent wafers tightly bonded while the white areas represent bubbles in interface. Almost no bubbles appear at the interface when annealed at 200 °C and 300 °C, except one that was caused by particle contamination. By contrast, when annealed at 400 °C slices separated and large areas of air bubbles are introduced, which is proved to be caused by the segregation of Sn from GeSn in high temperature. As shown in Fig. 2d, bonding strengths of the Ge/Si chips were evaluated by die shear test. 0.5 MPa of the Ge/GeSn/Si annealed at 200 °C and 2.13 MPa of the Ge/GeSn/Si annealed at 300 °C were obtained. In fact, during annealing process at 400 °C, the thermal stress induced in Ge/Si wafers is strong enough to spontaneously separate the bonding wafers from the bonding interface. Consequently, no die shear test was furtherly arranged.

The Ge/GeSn/Si wafers annealed at 300 °C has a good bonding strength. Figure 2e is the low-magnification TEM image, with its corresponding EDS mapping shown in Fig. 2f–h. Note that the Sn components are uniformly distributed in the GeSn layer and no segregation is observed on the surface. The average Sn content in the bonded immediate layer extracted from EDS results is about 5% in Fig. 2 L, which agrees well with the result calculating from sputtering power of the Ge: Sn ratio. For further investigation, Fig. 2i–k reveals the crystallization of a-GeSn thin films by HRTEM. The structural morphology at GeSn cross section can be divided into two regions, the large grained region (region I) and the fine nanocrystalline region (region II). In region I, a coherent interface was formed between GeSn film and Ge substrate along the (100) plane. The crystal area of GeSn grains range from 10 to 45 nm in the vertical direction. The SAED result further confirms that the GeSn grains are single crystal with a diamond cubic structure. The average lattice spacing of $Ge_{0.095}Sn_{0.05}$ was determined to be 0.328 nm, which is relatively close to the lattice spacing of bulk Ge. Comparing with Ge (0.326 nm) substrate, we can conclude the $Ge_{0.095}Sn_{0.05}$ layer is strained. In region II, nucleation near the Si substrate is observed, which will be analyzed in the following.

When the annealing temperature increased to 400 °C, the bonded Ge/GeSn/Si wafers separated. Figure 2 m shows the exposed GeSn film on Ge substrate after removing the Si slice. Some equilateral triangle dislocation pits along (111) formed, which ranges from 10 to 20 nm in depth confirmed by AFM. It's almost half the thickness of the film. From Fig. 2n and o, EDS results indicate that defects are formed during high annealing temperature due to the segregation and diffusion of β-Sn toward the film surface. As shown in Fig. 2p, when annealed at 200 °C, the exposed surface is relatively smooth. The Raman spectrum is featureless due to its amorphous nature. The wafers annealing at 300 °C is so high that bulk Ge slices are torn off from Ge substrate, which means that the maximum bond strength achieved is comparable to the bulk fracture strength of Ge substrates. Therefore, only single crystal Ge Raman peak is observed when annealing at 300 °C. Annealed temperature at 400 °C, the full width at half maximum (FWHM) of Ge-Sn peak from a-GeSn film decreases, close to the substrate peak of Ge. It fully turns to be single-crystal phase at the Ge/Si bonded interface. Moreover, the Ge-Sn peak is very close to the Ge peak, demonstrating that there is only a small amount of Sn atoms remained in Ge atoms matrix. From these results, a-GeSn as wafers bonding interlayer could crystallize after annealing in low temperature. However, annealing at high temperature, Sn tends to segregate from GeSn, leading to a deteriorated interlayer and failed Ge/Si bonding.

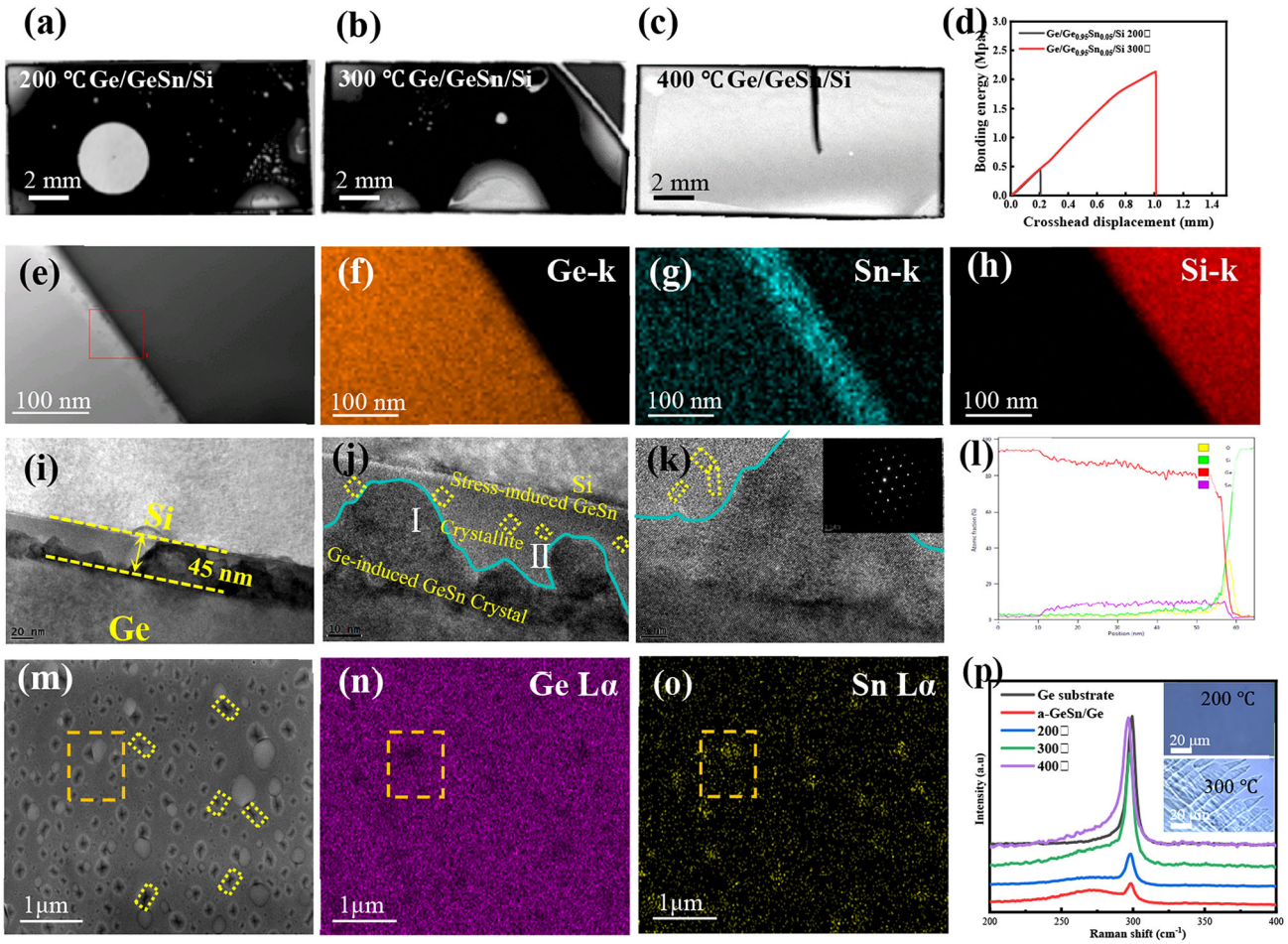

Fig. 2 CSAM images of the Ge/Si bonded wafer pairs with a 45 nm thick a-GeSn layer annealed at **a** 200 °C for 20 h, **b** 300 °C for 20 h. **c** 400 °C for 20 h. **d** Bonding strength of the Ge/Si bonded wafer pairs annealed at different temperatures. **e** TEM image of Ge/GeSn/Si interface annealed at 300 °C for 20 h with its EDS element mapping of the cross-section in **f**–**h**. **i**, **j**, **k** HRTEM images of the Ge/GeSn/Si bonded interface annealed at 300 °C for 20 h with its SAED pattern are shown in the upper right image in **k**. **l** The element distribution curve of the Ge/GeSn/Si bonded interfaces. **m** SEM images of the bonded interfaces of the Ge/GeSn/Si annealed at 400 °C for 20 h after the Si substrate removal, with its EDS element mapping shown in **n**, **o**. **p** Raman spectra of the GeSn interlayer annealed at 200 °C, 300 °C, 400 °C, respectively

To investigate the role of Sn in crystallization, a-Ge as an interlayer of Ge/Si bonding is carried out for comparison (Fig. 3a). TEM was also tested in Fig. 3b–d. From the fast Fourier transform pattern, the Ge interlayer remains amorphous. No evidence of crystallinity is observed. EDS element mapping of the cross-section is present in Fig. 3e–g, demonstrating an interlayer of pure Ge element. The bonding strength is 1.75 Mpa as shown in Fig. 3 h, which is lower than that of the Ge/GeSn/Si bonding sample. Based on the above results, without the introduction of Sn, a-Ge fails to crystallize at 300 °C. The crystallization temperature of a-Ge film can be drastically reduced by the introduction of Sn, which further validates the induction of Sn for formatting Ge crystalline grains. The acquired annealing temperature is just a little higher than the melting point of Sn (232 °C).

Besides, to study the formation mechanism of the nanocrystallites near Si substrate, it is required to exclude the influence of Ge substrate. Two Si/GeSn/Si bonding samples were annealed at 300 and 400 ° C, respectively. Raman spectra of these intermediate layers was collected to evaluate the crystallinity (Fig. 4a). The GeSn interlayer of Si/GeSn/Si annealed at 300 °C remains amorphous. Bonded samples after annealing at 400 °C were well crystallized; the intense

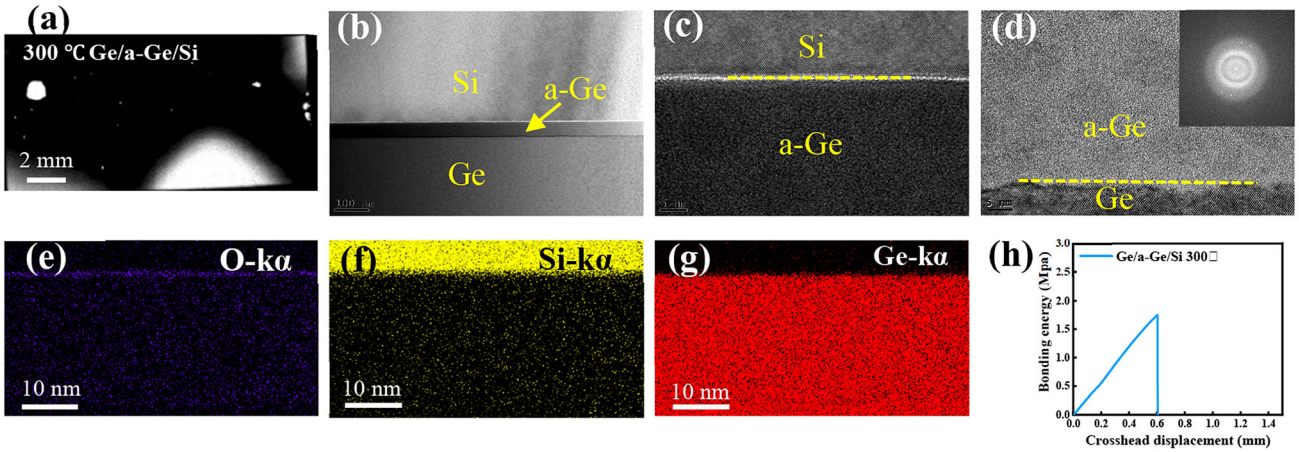

Fig. 3 **a** CSAM images of the Ge/Si bonded wafer pairs with a 45 nm thick a-Ge layer annealed at 300 °C for 20 h. **b–d** TEM images of the bonded interface of the Ge/a–Ge/Si annealed at 300 °C for 20 h and the fast Fourier transform (FFT) pattern taken from the same place at the top right. **e–g** EDS element mapping of the cross-section. **h** Bonding strength of the Ge/a–Ge/Si bonded wafers

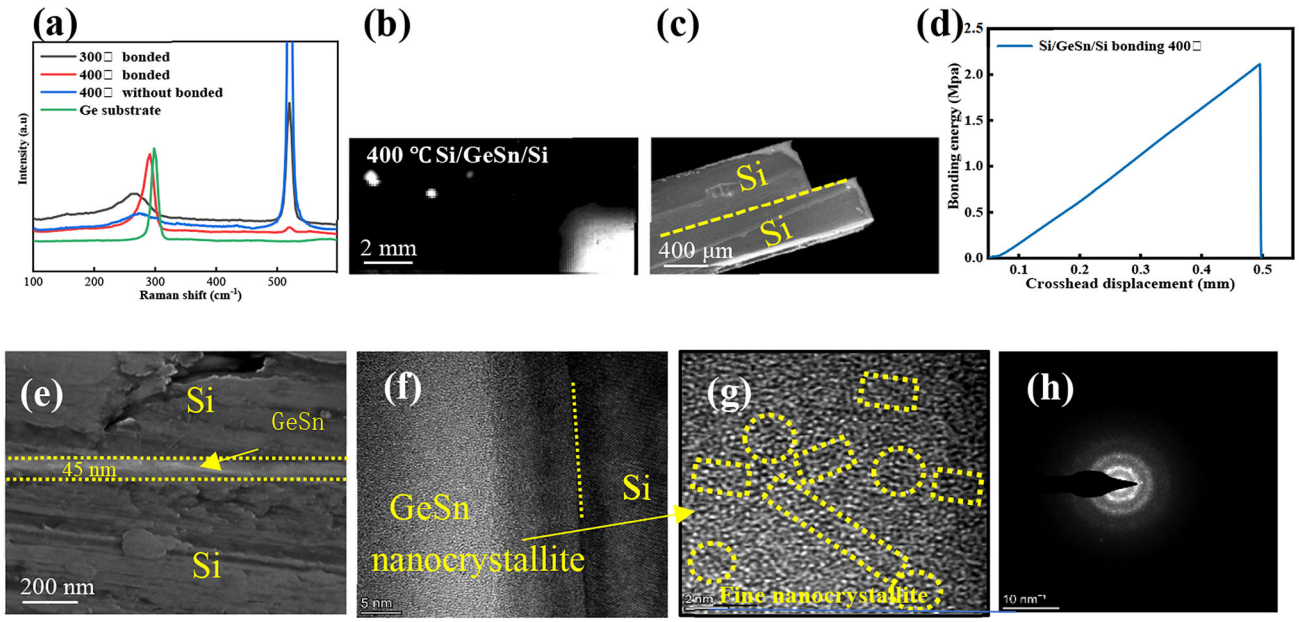

Fig. 4 **a** Raman spectra of the bonded interfaces of the Si/Si bonded wafer pairs. **b** CSAM images of the Si/Si bonded wafer pairs with a 45 nm thick a-GeSn layer annealed at 400 °C for 20 h. **c** Cross-section SEM images of Si/Si bonded wafer. **d** Bonding strength of the Si/GeSn/Si bonded wafer pair. SEM image (**e**) and HRTEM images (**f**, **g**) of the bonded interface of the Si/GeSn/Si annealed at 400 °C for 20 h. **h** The corresponding SAED pattern of the interlayer material in **g**; a ring with well-defined diffraction spots arising from the crystalline grains

and sharp phonon scattering peak present at 293 cm^{-1}. The blue shift of Ge–Ge phonon scattering can be attributed to Sn atoms replace with Ge [18] as well as in-plane strain ε caused by the thermal mismatch [19] between GeSn and Si substrate. For comparison, the GeSn/Si annealed at 400 °C was prepared. It has two broad phonon scattering peaks, which are the disparity of a-GeSn and Ge in 276 cm^{-1} and 302 cm^{-1} due to the disorder in the bond distances, demonstrating an amorphous phase. For further investigation, the Si/GeSn/Si in 400 °C was characterized by CSAM, cross section SEM and bond strength (Fig. 4b–d), revealing that GeSn has good adhesion to the substrate; no Sn segregation is

observed even at high temperature. As shown in Fig. 4e, a corner of Si/GeSn/Si is cut off by the grinding wheel and milled by focus-ion-beam (FIB). The GeSn intercalation is clearly observed to be sandwiched in the Si wafers. The TEM magnified image revealed the formation of fine nanocrystallites in Fig. 4f, g. Figure 4 h shows a SAED pattern taken from the nanocrystalline region, from which diffraction spots caused by nanocrystallites are visible. Notably, such nanocrystallites are similar to GeSn film near Si of Ge/Si wafers in 300 °C. Different from the crystallization of GeSn induced by Ge substrate, the crystallization of GeSn between Si substrate is probably induced by stress, which has been reported in previous works [20]. Theoretically, because of the thermal-expansion mismatch between GeSn film and Si wafers, a tensile-strain should be generated during cooling from high temperature to RT.

Considering the difficulty in measuring the strain field in the multilayered structures, finite element mechanical modeling is employed to further investigate the strain field distribution in Ge/GeSn/Si and Si/GeSn/Si. Thermal-structure coupling analysis is carried out on both Si/GeSn/Ge and Si/GeSn/Si through ANSYS Workbench. The deposited a-GeSn film on substrate was assumed to be stress-free before bonding, and the GeSn/Ge substrate was bonded onto another Si substrate with a pressure at room temperature (RT). For mechanical boundary conditions, the contact interfaces are bonded and the rest surfaces are set as free expansion. For thermal boundary conditions, the relaxation state at 300 °C is set as the initial state, and the RT is set to the final state. The involved material parameters are listed in Table 1 [21, 22]. The amorphous GeSn immediate layer is assumed isotropic and the coefficient of expansion of GeSn was calculated using linear interpolation [23].

Strain contours of Si/GeSn/Ge is shown in Fig. 5a. Vertical enlargement of the bonding structure shows that the intermediate layer has the maximum tensile strain. Ge substrate is hided in order to clearly study the normal strain distribution of GeSn film. To further analyze the strain variation in the bond structure, extract the strain along *Y*-axis as shown in Fig. 5b. The GeSn film in the middle is too thin to be seen relative to the 500 μm substrate, so a partial enlargement version of the middle section is shown in the top right corner.

Si/GeSn/Si is simulated in Fig. 5c. The simulation steps are similar to that in Ge/Si bonded sample, except that the relaxation state at 400 °C is set as the initial state. The maximum thermal strain located at GeSn interface turns to tensile strain in a sudden, while the Si substrate is subjected to a slight compressive strain as in Fig. 5d. Box in red is amplified as upper right corner of Fig. 5d. Strains on both sides of Si/Si bonded samples are symmetrically distributed, and a large tension strain is calculated in the GeSn layer.

Based on the simulation results, large tensile strain is generated in the interlayer of bonded wafers. For Ge/Si bonded wafers, when annealed at 300 °C, the atoms migration is accelerated and nucleation is promoted by Sn, resulting in the formation of GeSn grains. Then, under the influence of Ge substrate, GeSn single crystal was formed along the direction of the minimum free energy. For Si/Si bonded wafers, the strain on both sides is symmetric, which introduced by homogeneous structure. There is no crystallization at 300 °C due to the absence of Ge substrate. When annealed in 400 °C, Sn is still uniformly distributed, which is conducive to nucleation and nanocrystallites formation. As an accepted fact, the equilibrium solid solubility limit of Sn in Ge is less than 1%. With the Sn content increases in Ge, compressive stress is introduced and increases

Table 1 Material parameters for 3D-FEM simulation

Materials	Poisson's ratio	Young modulus (GPa)	Thermal expansion coefficient ($10^{-6}K^{-1}$)	Density (g/cm^3)
c-Ge	0.27	103	5.5	5.323
c-Si	0.28	130	2.6	2.392
a-Ge	0.27	91	7.9	5.0
α-Sn	0.298	51.53	4.7	5.75

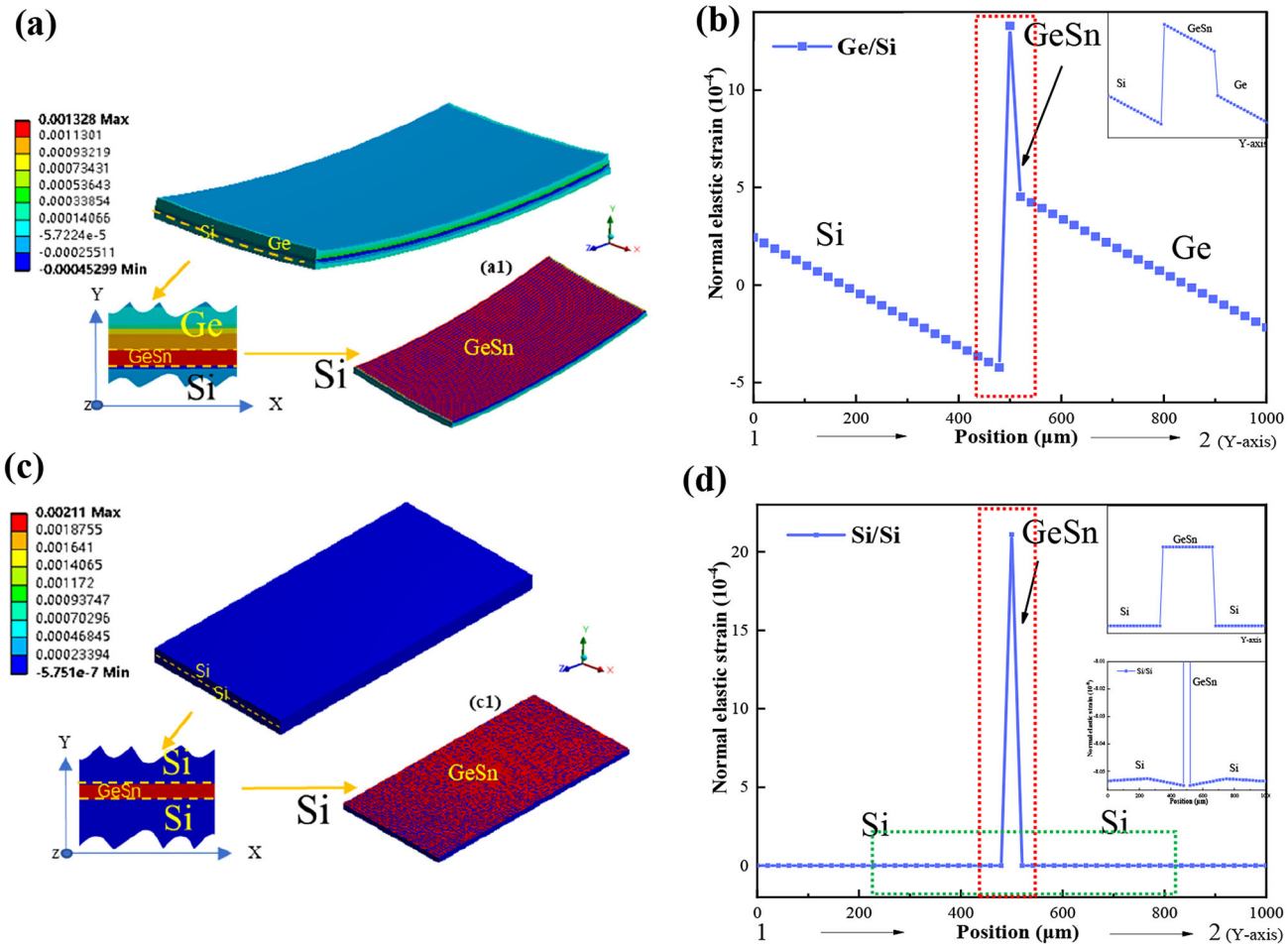

Fig. 5 The 3D FE model showing thermal-structure coupling analysis. Normal elastic strain of induced by **a** Ge/Si bonded wafers **c** Si/Si bonded wafers. Distribution of equivalent strain in the GeSn interlayer on Si (a1) (hiding Ge substrate), and in the GeSn surface film on Si (c1) (hiding one of the Si substrate). Interfacial strain distribution diagram of Ge/Si in **b**, Si/Si in **d**

constantly in Ge lattice. Excessive compressive strain prevents further incorporation of Sn [24, 25]. Nevertheless, our work proves that the sandwich structure can supply tensile strain to the GeSn interlayer, which is hopefully to balance the compressive strain in GeSn and thus further increase the solid solubility of Sn in Ge. Besides, the large strain plays an important role in triggering the nucleation and atoms rearrangement, and breaking the weaker bonds to reform stronger Ge–Sn bond [26], which contributes to decreasing crystallization temperature.

3 Conclusions

In conclusion, we have realized low temperature Ge/Si wafers bonding with a crystallized GeSn interlayer. On the one hand, the results of CASM and established tensile failure test proves the high strength Ge/Si heterojunction bonding and free of intrinsic voids after annealing at 300 °C. On the other hand, it turns out that a-GeSn is more easily crystallized in the strain field. This crystallization mechanism could provide some guidelines to synthesizing alloys with high composition and low solid solubility. Moreover, considering the potential implications for the integration of GeSn materials or GeSn devices on silicon, our work is promising to produce crystalline GeSn layer in the heterojunction for photonic applications and IV-group device.

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Availability of data and material

The data and material are available.

Declarations

Conflict of interest The authors declare no competing interest.

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